Synthesis of LC, RL and RC Circuit Using Embedded System Design Techniques

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Abstract
The paper is concerned with developing a soft-core processor system to be configured on Spartan 3E FPGA's slice using embedded design techniques. The developed processor system is accommodated to synthesize two-elements (LC, RL and RC) circuits based on the Partial Fraction expansion method. This work provides a suitable algorithm to realize analogue filters according their s-domain transfer function.

Keywords: Soft-core processor, FPGA, Embedded Development Kit (EDK), Partial Fraction expansion Method, LC, RL, RC, Spartan 3E

1. Introduction
Embedded system with Soft-core processors Possesses special advantages over custom designed processors such as tuned for low cost, Consumes minimum power, Hardware and software co-existence and Single-to fewer components based. FPGAs with configurable processor cores are a new, innovative approach to modern embedded system designs and open the door to hardware/software co-design and co-verification. Network synthesis involves the methods used to determine the structure of the electrical circuit and its component elements. Synthesizing two-element circuits using partial fraction method produces LC, RL and RC circuits depending on the transfer function[Kuo1966]as described in the following equation(1):

$$F(s) = \frac{\alpha_0 s^n + \alpha_1 s^{n-1} + \cdots + \alpha_n}{\beta_0 s^n + \beta_1 s^{n-1} + \cdots + \beta_n}$$  (1)

In order to synthesize a driving point function into a passive network it must be positive real (p.r) and satisfy the constraints of stability and causality with the following properties [SONAL 07].

i. It must be rational function of the complex frequency, s.

ii. The poles must lie on the left hand side of the jw axis or on the imaginary axis (stable function).

iii. The poles on the jw axis must be simple. The denominator polynomial must be Hurwitz.

iv. Complex poles and zeros must occur in conjugate pairs.
Alexander J. Casson and Esther Rodriguez-Villegas presents proposed a methodology for the design of doubly terminated LC ladder structures making use of the symbolic maths engines in programs such as MATLAB and MAPLE. But this methodology is explained only LC ladder type [Alexander J. Casson, 2011]. Grimbleby has employed a hybrid-Genetic Algorithm (GA) approach to synthesize circuits for frequency-domain and time-domain specifications. But the circuits generated are efficient in the sense of using the minimum number of components and are often generating designs with complexity of 10-20 components in hours [GRIMBLEBY, J.B., 2000].

This work aims to design an embedded processor system that can be programmed to synthesize LC-RC-RL circuits according to their s-domain transfer functions this process is characterized by simplicity, efficiently and speed.

The design procedure includes explaining the principles of embedded design techniques and the construction of the processor system, synthesis system and partial fraction expansion circuit, results and discussion.

2. Embedded Design Techniques

The soft-core processor system design procedure includes the development of hardware and software parts. The embedded processor based system is configured on spartan3E500 starter kit using Embedded Development Kit (EDK). (EDK) is a collection of tools and Intellectual Properties (IP's) that uses Xilinx Platform Studio (XPS) for designing the software and hardware platform developments. The designed system is composed of hardware part and software part.

The hardware part consists of MicroBlaze soft-core processor with its associated busses, Dual Data Rate - Synchronous Dynamic Random Access Memory (DDR-SDRAM) with its Multi-Port Memory Controller (MPMC) on PLB port, and I/O devices controllers such as Universal Asynchronous Receiver Transmitter (UART) Controller; the hardware platform is saved in the Microprocessor Hardware Specification (MHS) file [Xilinx. Inc 08].

The software part is a collection of software drivers and the operating system on which the application is built. The embedded software platform defines the drivers associated with the peripherals included in hardware platform, selected libraries, standard input/output devices, interrupt handler routines, and other related software features, it also defines software applications to be run on processor, the software platform is saved in the Microprocessor Software Specification (MSS) file [Xilinx. Inc 08]. MSS file together with software applications, are the principal source files that represent the software component of embedded system.

The hardware system is programmed using C language with which an application program was developed. Figure (1) provides an overview of the embedded system design techniques [Xilinx. Inc 10].
3. CIRCUIT SYNTHESIS ALGORITHMS

Network synthesis involves the methods used to determine an electric circuit that satisfy certain specifications. In the synthesis of networks, the most commonly preferred synthesis methods are the two-element synthesis methods [SONAL 07]. Synthesis is performed using the classical technique which is based on partial fraction expansion method.

The basic philosophy behind the synthesis of driving-point functions is to break up a p.r. function $Z(s)$ into a sum of simpler p.r. functions $Z_1(s), Z_2(s)... Z_n(s)$, and then to synthesize these individual $Z_i(s)$ as elements of the overall network whose driving-point impedance is $Z(s)$ as described in equation bellow [Kuo 1966]

$$Z(s) = Z_1(s) + Z_2(s) + ... + Z_n(s)$$  \hspace{1cm} (2)

One important restriction is that all $Z_i(s)$ must be p.r. The transfer function may be in the form of admittance $Y(s)$.

3.1. LC circuit
The properties of the transfer function of LC circuit are: ZLC(s) or YLC(s) is the ratio of odd to even or even to odd polynomials, The poles and zeros are simple and lie on the jw axis, The poles and zeros interlace on jw axis, The highest powers of numerator and denominator must differ by unity; The lowest powers also differ by unity and There must be either a zero or a pole at the origin and infinity. The partial fraction expansion of LC function is expressed in the form [Kuo 1966]

\[ F(s) = \frac{k_0}{s} + \frac{2k_2}{s^2 + w_2^2} + \ldots + k_w s \]  

(3)

3.2. RC Impedance and RL Admittance

The properties of RC impedance are the same as those of RL admittance, hence RC impedance can also be realized as an RL admittance. The properties are: The poles and zeros are real and lie on the negative real axis, they alternate, the singularity nearest to (or at) the origin must be a pole whereas the singularity nearest to (or at) \( \sigma = -\infty \) must be a zero and the residues of the poles must be real and positive. The partial fraction expansion of RC impedance or RL admittance function is expressed in the form [Kuo 1966]

\[ F(s) = \frac{K_0}{s} + K_w + \frac{K_1}{s + \sigma_1} + \ldots \]  

(4)

3.3. RL Impedance and RC Admittance

The properties of RL impedance are the same as those of RC admittance, hence RL impedance can also be realized as an RC admittance. The properties are: The poles and zeros of an RL impedance or RC admittance are located on the negative real axis, they alternate, the singularity nearest to (or at) the origin is a zero, the singularity nearest to (or at) \( s = -\infty \) must be a pole and the residues of the poles must be real and negative. The admittance that represent RL impedance or RC admittance is expressed in the form [Kuo 1966] as bellow

\[ F(s) = K_w s + K_0 + \frac{K_1 s}{s + \sigma_1} + \ldots \]  

(5)

Because of the third property the partial fraction expansion of RL impedance will yield terms in the form \( \frac{K_1 s}{s + \sigma_1} \) which does not represent an RL impedance or RC admittance at all. This problem is solved by divide the function F(s) by "s", the partial fraction expansion of F(s)/s will yield positive residue, thus we have

\[ \frac{F(s)}{s} = K_w + \frac{K_0}{s} + \frac{K_1}{s + \sigma_1} + \ldots \]  

(6)

Where \( k_0, k_1, k_2 \ldots k_w \geq 0 \)

Multiplying both sides of equation (6) by "s", F(s) in the desired form for the synthesis is obtained.

4. Developing soft-core processor system

Figure (2) shows the assembly view issued by Xilinx platform studio [Xilinx. Inc 10], for the developed soft-core processor system.
Figure (3) shows the address map of the developed system.

![Address Map](image)

**Fig. (2) The assembly views of soft-core system.**

![Assembly Views](image)

**Fig. (3) The address map of the developed system.**

5. Synthesis Technique (algorithm)

The designed embedded processor system is programmed using C language to perform synthesis operation. Figure (4) shows the flow chart of synthesis algorithm. This clever algorithm identifies the type of the circuit and its components from a given transfer function according to the properties of the function.

In order to synthesize a network from a given system transfer function, the following steps are adopted:

1. Define the variables $N_1, N_2$ to represent the number of nonzero coefficient in the numerator and denominator respectively.
2. Define the variables $L_1, L_2$ to represent the lower exponent in the numerator and denominator respectively.
3. Store in ascending order the numerator coefficient and corresponding exponent of "s" in a matrix named (b_NUM).
4. Store in ascending order the denominator coefficient and corresponding exponent of "s" in a matrix named (a_DEN).
5. Defining the type of transfer function to be "Z" for impedances and "Y" for admittance.
6. Find the poles and zeros of the given transfer function by finding the roots of denominator and numerator using Bairstow's method [Steven 02].
7. Check the simplicity of the pole and zeros.
8. Check the location and alternation of the real root on negative real axis by algorithm in Figure (5).
9. Check the interlace of the imaginary roots on jw axis by the same algorithm in Figure (5).

**Fig .(4) The flow chart of the synthesis Program**

10. Check that highest (and lowest) power of the denominator differ by unity.
11. Perform partial fraction expansion and determine the residues of the poles.
12. Comparing the data collected from the above mentioned steps with the properties of two-element circuit, the type of the circuit representing the given function can be discovered.
6. RESULTS

The performance of the designed system is tested for synthesizing the following transfer function.

\[ Z(s) = \frac{s^3 + 20s^3 + 64s}{s^5 + 259s^3 + 185s^2 + 225} \quad (7) \]

\[ Y(s) = \frac{s^2 + 8s + 12}{s^2 + 6} \quad (8) \]

\[ Y(s) = \frac{3s^2 + 10s + 24}{s^2 + 3s} \quad (9) \]

\[ Z(s) = \frac{3s^2 + 10s + 24}{s^2 + 3s} \quad (10) \]

Figure (6) displays the synthesis result of the transfer function described by equation (7). Figure (6.a) shows the synthesis result on the HyperTerminal window, the circuit is LC Impedance type with the values of its components are shown. Figure (6.b) exhibits the structure of the circuit.
Fig. (6) Synthesizing result of equation (7)

(a) The result displayed on the HyperTerminal window.
(b) The structure of the synthesized Circuit.

Figure (7) displays the synthesis result of the transfer function described by equation (8). Figure (7.a) shows the synthesis result on the HyperTerminal window, the circuit is RC Admittance type with the values of its components are shown. Figure (7.b) exhibits the structure of the circuit.

Fig. (7) Synthesizing result of equation (8)

(a) The result displayed on the HyperTerminal window.
(b) The structure of the synthesized Circuit.

Figure (8) displays the synthesis result of the transfer function described by equation (9). Figure (8.a) shows the synthesis result on the HyperTerminal window, the circuit is RL Admittance type with the values of its components are shown. Figure (8.b) exhibits the structure of the circuit.
(a) \hspace{2cm} \text{Fig. (8) Synthesizing result of equation (9)}
\hspace{2cm} a . \text{The result displayed on the HyperTerminal window.}
\hspace{2cm} b . \text{The structure of the synthesized Circuit.}

Figure (9) displays the synthesis result of the transfer function described by equation (10). Figure (9.a) shows the synthesis result on the HyperTerminal window, the circuit is RC Impedance type with the values of its components are shown. Figure (9.b) exhibits the structure of the circuit.

(b)

(b)

\hspace{2cm} \text{Fig. (9) Synthesizing result of equation (10)}
\hspace{2cm} a . \text{The result displayed on the HyperTerminal window.}
\hspace{2cm} b . \text{The structure of the synthesized Circuit.}

Conclusions

An Embedded designed processor system can be designed and adapted to be used in synthesizing two-element circuit. The work developed an algorithm for synthesizing LC, RL and RC circuits with the aid of soft-core processor system; this initiates a novel algorithm for FPGAs based synthesis algorithm which is necessary in analogue filter realization process. The developed processor system is harnessed to synthesize passive elements circuits based on the Partial Fraction expansion method. The motivation behind this research is to automate the process of network synthesis, making it
simple, efficient and fast, leading to an essential application of FPGA based circuit design.

References: